## ABSTRACT OF THE DISCLOSURE

Embodiments of the invention include a trio of reliability oscillators. In one embodiment, an on-chip frequency compensation circuit includes a selectively enabled reliability oscillator to generate a reference oscillating signal, a clocked reliability oscillator to generate an AC degraded oscillating signal, and a static reliability oscillator to generate a DC bias degraded oscillating signal. A compare circuit coupled to the reliability oscillators compares the oscillating signals and generates a frequency compensation signal if the comparison determines that there is frequency degradation greater than a predetermined threshold.